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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,891	10/11/2005	Chiu Hao Cheng	CHEN3516/REF	4442

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EXAMINER	
RADOSEVICH, STEVEN D	
ART UNIT	**PAPER NUMBER**
2117	
MAIL DATE	**DELIVERY MODE**
10/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,891	CHENG ET AL.	
	Examiner	Art Unit	
	STEVEN D. RADOSEVICH	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *1-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-31* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-31 are present within this initial examination. Examiner notes claims 1-18 are canceled by applicant and will not be given further consideration.

Priority

Acknowledgment is made that priority for this application is to 4/8/2003 which is the PCT filing date of PCTUS0309201.

Information Disclosure Statement

Acknowledgment is made that an Information Disclosure Statement (IDS) was filed prior to this initial examination, disclosing two documents, a U.S. Patent document and a Foreign Patent document. At this time acknowledgment is made that these documents have been fully considered and therefore the IDS has been fully reviewed at this time.

Drawings

Acknowledgment is made that the figures do not appear at this time to have any issues that would require and objection and/or correction by the applicant, and therefore are accepted as they appear when submitted on 10/11/2005.

Claim Objections

Claim 30 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Examiner notes that, that which is claimed in claim 30 is identical to the last limitation of claim 29, from which

claim 30 is dependent upon. Furthermore examiner notes that it is believed applicant indented to follow the format of claims 19-22 and 26-28 with respect to claim 23-25, when writing claims 29-31; wherein the claim 20 limitation is incorporated within the independent claim 18 limitations such is the case with claim 23 without a depending claim adding the limitation, thus reducing the number of dependent claims. The limitation of claim 30 is fully considered within that which constitutes claim 29 and therefore may not be given further consideration within this examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 19-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Veenstra et al. (U.S. Patent 6460148) and further in view of Noguchi (U.S. Patent 4730314).

1. As per claims 19 and 26, Veenstra teaches a logic analyzer comprising the steps of:

Providing and storing a time delay value in said buffer of said time delay circuit (310 in figure 8 and column 14 lines 10-25, and column 19 lines 45-50);

Presetting at least a clock qualifier signal based on a specific parameter (qualifiers in column 26 lines 50-60, trigger condition in column 3 lines 30-40);

Triggering a preset of said first counter and transferring said default value from said buffer to said first counter to drive said first counter to start counting in response to said clock qualifier signal until said delay default is reached (set delay and Triggered in figure 8, column 17 lines 50-65, and column 18 lines 50-65); and

Capturing test data from a test sample electrically connected to the logic analyzer in response to said triggering of said preset of said first counter until said first counter counting reaches said delay default value, wherein said control unit is adopted for capturing said test data from a test sample (signal to be captured in column 18 lines 50-60, and “capturing sample data”, “captured signals”, and “capture” in column 19 lines 1-50).

Veenstra does not specifically teach the logic analyzer comprising a step of triggering a preset of said second counter, in response to said first counter counting reaching said delay default value, to start counting until the preset of the first counter is triggered again.

However Noguchi teaches wherein a logic analyzer triggers a preset of a second counter, in response to a first counter counting reaching a delay default value, to start counting until the preset of the first counter is triggered again (46 and 45 in figure 4, column 5 lines 45-68).

Therefore one of ordinary skill within the art at the time the invention was made would have been motivated to modify Veenstra to incorporate the further counting of Noguchi, wherein a second counter is preset and counts until the preset and counting of the first counter, to provide a logic analyzer a clear indication of the time or temporal relationship between input data available form a plurality of analysis sections operating on different sampling clocks as disclosed within Noguchi (column 3 lines 64-68).

2. As per claims 20, 23, 27, and 29-30, Noguchi teaches wherein counting value of said second counter is stored in said memory unit when said second counter stops counting and then displaying the value on a display screen (48 and 49 in figure 4 along with 37 in figure 4).

3. As per claims 21 and 24, Veenstra teaches further comprising a step of sampling clock input only during the period of a clock enable signal (Enable in figure 8, qualifiers in column 26 lines 50-60, trigger condition in column 3 lines 30-40).

4. As per claims 22 and 25, Noguchi teaches wherein an output of said clock enable signal is a low when said first counter starts counting, and the output of said clock enable signal is high when said first counter counted until said default value is reached (column 5 lines 45-68 and figure 4).

5. As per claims 28 and 31, Veenstra teaches further comprising a trigger assembly logic circuit capable of receiving multiple test signals from multiple test samples (302 in figure 8).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. Marantz et al (U.S. Patent 6061511) discloses within a logic analyzer multiple capture times wherein the time duration between capture times is counted (see figure 10 and column 8 line 61 – column 9 line 15).

ii. Dervisoglu et al (U.S. Patent 6687865) discloses within a logic analyzer a stop counter and address counter wherein the counter is loaded with a value equal to the memory size in-order to prevent overflow.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN D. RADOSEVICH whose telephone number is (571)272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JACQUES H LOUIS-JACQUES/
Supervisory Patent Examiner, Art Unit 2100

Steven D. Radosevich
Examiner
Art Unit 2117